AMENDMENTS TO THE SPECIFICATION

Please amend the specification as indicated hereafter. It is believed that the following amendments and additions add no new matter to the present application.

Please replace the paragraph starting on p. 5, line 8 with the following amended paragraph:

The first IC 102 comprises a first contact 104 labeled V_{DD} via which an amount of power is provided that is appropriate to power the first IC 102. Transmit logic 106 is also located within the first IC 102 for purposes of transmitting data from the first IC 102 to the second IC 132, wherein the data may be stored within a storage (not shown). Transmission of the data is performed via a first transmit contact 108 that is connected to a second receive contact 134 located within the second IC 132. Data transmitted from the second IC 132 to the first IC 102 is received via a first receive contact 112 and transmitted to receive logic 114 located within the first IC 102. Receive logic [[144]] 114 is further described herein with reference to FIG. 2.

Please replace the paragraph starting on p. 8, line 5 with the following amended paragraph:

Setup time is the minimum time required for a data signal received at the register 172 to be stable before the arrival of an edge of a clock signal, rising or falling, depending on the type of register 172, changes the state of the register 172. For explanation purposes, the following description assumes that the register 172 responds to rising edges of clock signals. Specifically, the register 172 analyzes and stores received data during a required setup time. Unfortunately, if the rising edge of a clock signal is not received during the setup time of the register 172, the register 172 stops storing data and the data is lost. Further, if the setup time is too long, then new data may be received prior to completion of initial data storage. Therefore, if the setup time is ignored, unpredictable behavior by the register 172 can be expected. This unpredictable behavior manifests in several ways including, but not limited to, missed data or ignored actions, and possible partial transient outputs of the register 172.

Please replace the paragraph starting on p. 9, line 10 with the following amended paragraph:

As is shown by block 202, the setup and hold times of the receive logic 144 are minimized. ~~A miniaturized version~~ Miniaturized versions of the clock buffer 176 located within the clock path [[is]] are then fabricated (block 204). As is shown by block 206, the miniaturized versions of the clock buffer 176 are then placed within the data path to the register 172. Variations in process, voltage and temperature experienced by the clock buffer 176 are then minimized (block 208). Each of these steps is described in detail below.

Please replace the paragraph starting on p. 10, line 4 with the following amended paragraph:

The setup and hold times of the receive logic 144, T_{setup} and T_{hold} respectively, may be expressed in terms [[a]] of a delay attributed to the clock receiver 174 ($T_{clk\text{-}rcv}$), clock buffer 176 ($T_{clk\text{-}dly}$), data receiver 182 ($T_{data\text{-}rcv}$), data delay device 184 ($T_{data\text{-}dly}$), and propagation of the clock signal ($T_{clk\text{-}rte}$). Equation one, provided below, demonstrates the setup time of the receive logic 144 in terms of delay.

Please replace the paragraph starting on p. 12, line 20 with the following amended paragraph:

FIG. 4 is a block diagram further illustrating receive logic 144 comprising a first and second miniature clock buffer 192, 194 in the data path equal to the number of clock buffers 176 located in the clock path. It should be noted that any circuit fabrication software may be utilized to design the miniature clock buffers 192, 194 by scaling down the size of the original clock buffer 176. The miniature clock buffers 192, 194 are a scaled down version of the original clock buffer 176 because the original clock buffer 176 is too large and consumes too much power to simply be placed in the data path. If the clock buffer 176 were introduced into the data path for delay purposes, noise ~~being~~ would be introduced into the data path since excess voltage is needed to power the clock buffer 176.

Please replace the paragraph starting on p. 13, line 22 with the following amended paragraph:

Unfortunately, temperature variations, which add approximately ten percent of uncertainty to circuit timing, are not currently capable of being compensated for. Therefore, the delay contributed by the clock buffer 176 is multiplied by one hundred ten percent ~~(.1)~~ (1.1) to account for this variation. The resulting setup and hold delays for the receive logic 144 are shown by equations five and six provided hereinbelow.

Please replace equations 5 and 6 on p. 13, lines 4 and 5 with the following amended formulas:

$$T_{setup} = T_{reg\text{-}setup} + \sim\!\!0.1\!\!\sim\ 1.1 \times (-T_{clk\text{-}dly}) - T_{clk\text{-}rte}(min) \qquad \text{(Eq. 5)}$$

$$T_{hold} = T_{reg\text{-}hold} + \sim\!\!0.1\!\!\sim\ 1.1 \times (T_{clk\text{-}dly}) + T_{clk\text{-}rte}(max) \qquad \text{(Eq. 6)}$$